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CLAIMS

What is claimed is:

1. A process for fabricating a complementary metal oxide semiconductor (CMOS) structure comprising:

providing a plurality of polySi gates overlying a semiconductor substrate, each polySi gate comprises a dielectric cap located on an upper surface thereof;

forming silicided source/drain regions in the semiconductor substrate;

forming a planarized dielectric stack on the semiconductor substrate;

performing an etching process to selectively remove the dielectric cap against polySi and thereby expose an upper surface of each polySi gate, wherein the etching process does not etch the polySi gates, so that the exposed polySi gates formed by the etching process have substantially the same height; and

performing a salicide process which converts each polySi gate to a metal silicide gate, wherein each metal silicide gate has substantially the same height, is composed of the same silicide phase, and has substantially the same workfunction for the same polySi ion implant conditions.

2. The method of Claim 1 wherein the plurality of polySi gates are formed atop a gate dielectric.
3. The method of Claim 1 wherein the plurality of polySi gates are formed by deposition, lithography and etching.
4. The method of Claim 1 wherein the dielectric cap comprises Si₃N₄.

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5. The method of Claim 1 wherein the step of providing the plurality of polySi gates includes the formation of at least one spacer on each exposed sidewall of the polySi gates.
6. The method of Claim 5 wherein the at least one spacer includes a first spacer and a second spacer, wherein the first spacer has a thickness that is narrower than the second spacer.
7. The method of Claim 1 wherein the step of forming the silicided contacts on source/drain regions comprises depositing a metal atop the semiconductor substrate, and performing a salicide process.
8. The method of Claim 7 wherein the metal comprises Ti, Ta, W, Co, Ni, Pt, Pd or alloys thereof.
9. The method of Claim 8 wherein the metal is Co, Ni or Pt.
10. The method of Claim 7 wherein the salicide process comprises a first anneal, a selective etching step and optionally a second anneal.
11. The method of Claim 7 further comprising forming a layer of silicon atop the semiconductor substrate prior to metal deposition.
12. The method of Claim 1 wherein the step of forming a planarized dielectric stack comprises deposition and planarization.
13. The method of Claim 1 wherein the step of forming a planarized dielectric stack comprises forming an etch step layer, forming an interlevel dielectric and planarizing the interlevel dielectric.
14. The method of Claim 1 wherein the etching process comprises a reactive ion etch step.

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15. The method of Claim 1 wherein the salicide process comprises depositing a blanket silicide metal layer atop the at least the exposed upper surface of each polySi gate, first annealing to cause total or partial consumption of the polySi gates, selective etching non-reacted silicide metal and optionally performing a second anneal.

16. The method of Claim 15 wherein the silicide metal comprises Ti, Ta, W, Co, Ni, Pt, Pd or alloys thereof.

17. The method of Claim 16 wherein the silicide metal is Co, Ni or Pt.

18. The method of Claim 15 the first anneal is performed at a temperature from about 350° to about 550°C.

19. The method of Claim 15 wherein the optional second anneal is performed at a temperature from about 600°C to about 800°C.

20. A method of forming a CMOS structure having silicide contacts comprising the step of:

providing a structure comprising a plurality of polySi gates overlying a semiconductor substrate;

depositing a silicide metal directly atop the structure including the polySi gates and the semiconductor substrate;

forming a recessed, reflow material between each polySi gate;

selectively removing silicide metal from atop each of the polySi gates by using an etching process to expose an upper surface of each of the polySi gates, wherein the etching process does not etch the polySi gates, so that the exposed polySi gates formed by the etching process have substantially the same height;

removing the recessed, reflow material; and

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annealing the structure so as to form silicide contact regions between each of the polySi gates.

21. The method of Claim 20 wherein the silicide metal comprises Ti, Ta, W, Co, Ni, Pt, Pd or alloys thereof.

22. The method of Claim 21 wherein the metal is Co, Ni or Pt.

23. The method of Claim 20 wherein the recessed, reflow material comprises an antireflective coating or a spin-on dielectric.

24. The method of Claim 20 wherein the forming the recessed, reflow material comprises deposition and optional etching.

25. The method of Claim 20 wherein the removing the silicide metal comprises a wet etching process that uses a sulfuric acid/hydrogen peroxide solution.

26. The method of Claim 20 wherein the annealing includes at least a first annealing step which is performed at a temperature from about 300°C to about 600°C.

27. The method of Claim 26 further comprising an optional second annealing step which is performed at a temperature from about 600°C to about 800°C

28. The method of Claim 20 further comprising forming metal silicide gates by depositing and planarizing a capping bilayer comprising SiO₂ and Si₃N₄; performing an optional wet etch process to remove SiO₂; performing a selective RIE process to remove Si₃N₄ atop the gate; forming a silicide metal on the gate; and performing a salicide process.

29. A method of forming a CMOS structure having silicide contacts comprising the step of:

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providing a structure comprising a plurality of polySi gates overlying a semiconductor substrate;

forming a bilayer layer comprising a metal layer and a capping layer directly atop the structure including the polySi gates and the semiconductor substrate;

forming a planarizing material on the semiconductor substrate;

exposing the metal layer atop each polySi gate;

selectively removing the metal layer from atop each polySi gate by utilizing an etching process to expose an upper surface of each of the polySi gates, wherein the etching process does not etch the polySi gates, so that the polySi gates formed by the etching process have substantially the same height;

removing the planarizing material; and

annealing the structure so as to form silicide contact regions between each of the polySi gates.

30. The method of Claim 29 wherein the metal layer comprises Ti, Ta, W, Co, Ni, Pt, Pd or alloys thereof.

31. The method of Claim 30 wherein the metal layer is Co, Ni or Pt.

32. The method of Claim 29 wherein the capping layer comprises TiN, W or Ti.

33. The method of Claim 29 wherein the planarizing material comprises a photoresist or a low temperature oxide.

34. The method of Claim 29 wherein the exposing comprises chemical mechanical polishing of the planarizing material and etching of the capping layer.

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35. The method of Claim 29 wherein the removing of the metal layer from atop each polySi gate includes a wet etching process using a sulfuric acid/hydrogen peroxide solution.
36. The method of Claim 29 wherein the annealing includes at least a first annealing step which is performed at a temperature from about 300°C to about 600°C.
37. The method of Claim 36 further comprising an optional second annealing step which is performed at a temperature from about 600°C to about 800°C
38. The method of Claim 29 comprising forming metal silicide gates by depositing and planarizing a capping bilayer comprising SiO₂ and Si₃N₄; performing an optional wet etch process to remove SiO₂; performing a selective RIE process to remove Si₃N₄ atop the gate; forming a silicide metal on the gate; and performing a salicide process.